UNIVERSITY OF EDUCATION, WINNEBA

COLLEGE OF TECHNOLOGY EDUCATION, KUMASI

A SIMPLE DESIGN METHOD FOR NONLINEAR CONTROL OF POWERFACTOR CORRECTION BOOST CONVERTER

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A Dissertation in the DEPARTMENT OF ELECTRICAL AND AUTOMOTIVE TECHNOLOGY EDUCATION, Faculty of TECHNICAL EDUCATION, submitted to the School of Graduate Studies, University of Education, Winneba in partial fulfillment of the Requirement for the award of the Master of Technology Education (Electrical/Electronic Technology) degree.

DECEMBER, 2016

DECLARATION

STUDENT'S DECLARATION

I, **ASAPH AGYEI MENSAH**, declare that this Dissertation, with the exception of quotation and reference contained in published works which have all been identified and duly acknowledged, is entirely my own original work, and it has not been submitted, either in part or whole, for another degree elsewhere.

SIGNATURE ……

DATE**:** …….

SUPERVISOR'S DECLARATION

I hereby declare that the preparation and presentation of this work was supervised in accordance with the guidelines for supervision of Dissertation as laid down by the University of Education, Winneba.

NAME OF SUPERVISOR: PROFESSOR WILLIE K. OFOSU

SIGNATURE: ……

DATE:……

ACKNOWLEDGEMENT

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I would like to express my gratitude to Professor Willie K. Ofosu for guidance and support throughout this project work. He has been a constant source of inspiration to me throughout the period of this work. I consider myself extremely fortunate for having the opportunity to learn and work under his supervision over the entire period.

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I thank all my classmates for their encouragement and help.

DEDICATION

This work is dedicated to my family and the entire staff of Srebuoso D/A JHS

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ABSTRACT

Typical switched-mode power supplies employ diode rectifiers for the AC to DC conversion. They draw input current in short pulses rather than in smooth sine waves and this puts stress on the wiring, circuit breakers and even distribution equipment provided by utilities. This type of utility interface generates harmonics and both of the input power factor (PF) and total harmonic distortion (THD) are poor. To minimize the stresses and maximize the power handling capabilities, active power factor correction (PFC) circuitry can be added to improve the shape of the input current. This work is aimed at providing a simple design method for power factor correction (PFC) boost converter for a non-linear power system to improve the disturbance rejection and speed of response of the conventional nonlinear cascade controller. Model based cascade controller design is presented for the control of PFC boost converters. Also, a dead band relay is introduced in the voltage loop to improve the disturbance rejection and speed of response of the PFC boost converter. Circuit implementation of the proposed control scheme is presented and simulation results are included to demonstrate the effectiveness of the proposed design scheme. The outcome indicated that resultant power factor is over 0.99, the total harmonic distortion of supply current is less than 2.9% and the efficiency of the converter is 93% at full load. It is recommended that a MOSFET based switching device could be used to improve the system.

CHAPTER ONE

INTRODUCTION

1.1 Background to the Study

Typical switched-mode power supplies employ diode rectifiers for the AC to DC conversion. They draw input current in short pulses rather than in smooth sine waves (Chan et al., 1997) and this puts stress on the wiring, circuit breakers and even distribution equipment provided by utilities. This type of utility interface generates harmonics and both of the input power factor (PF) and total harmonic distortion (THD) are poor [Chan et al., 1998]. To minimize the stresses and maximize the power handling capabilities, active power factor correction (PFC) circuitry [Singh et al., 2003; Garcia et al., 2003] can be added to improve the shape of the input current. The boost converter based topology, which is a combination of bridge rectifier and step-up boost converter, is widely used because of the simple gate drive circuit, high efficiency and small input inductor [Sahid et al., 2003]. The boost PFC converters provide well-regulated DC output voltage even under wide varying AC input voltage from 85 V to 265 V. They are extensively used in electronic ballasts, switching mode power supplies and variable speed drives. For medium and high power single-phase PFC, continuous conduction mode (CCM) is preferred due to its high efficiency and low current stress in semiconductor components. The UC3854 [Todd et al.] uses average current mode control to accomplish fixed frequency current control with stability and low distortion. Unlike peak current mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients. Although the average

current mode method uses analogue multiplier that increases the complexity and cost of control circuitry, much research has been dedicated to PFC control method for the CCM operation without a multiplier [Maksimovic 1996; Maksimovic 1995; Lai et al., 1998]. In the conventional CCM topology, there are two control loops. They are the voltage loop, which is used to regulate the output voltage, and the current loop, which is used for the control of the input current. PFC voltage loops are normally implemented with low bandwidth [Yang et al., 1998] in order to reduce the AC ripple on the output voltage, which distorts the input current waveform. Also, in the case of step load change, the controller cannot response fast enough, and this leads to large voltage overshoot. In addition to the analogue based proportional–integral–derivative control, advanced control methods, such as sliding mode control [Lopez et al., 2001], fuzzy logic control [Chung et al., 1999], and neural network control [Simonetti et al., 1993], are also employed to provide fast dynamic response while maintaining the stability of the converter system over a wide operating range. However, most of them are digitally controlled and they require expensive and fast digital signal processors to implement. References [Prodic et al., 2004; Orabi et al., 2002] present some results on the stability issues of PFC converters due to its nonlinear behaviors.

To improve the speed of response and to improve the disturbance rejection of conventional analogue controlled boost converters, a proposed nonlinear dead-band relay is added to the conventional controller to enhance the dynamic response. To facilitate low cost analogue nonlinear control, nonlinear cascade control of PFC boost converter is proposed. Simple proportional plus integral controllers can easily be designed based on

the state average model of the boost converter. The overall design will compose of two control loops with the voltage loop outside the inner current loop. As long as the dynamics of the inner current loop is much faster than the outer voltage loop, cascade control can be implemented. To achieve a high power factor and low current THD, the bandwidth of the current loop has to be sufficiently fast to track the power frequency as well as its higher harmonics. At the same time, the current loop must have sufficient attenuation to reduce the effect of supply voltage and output regulated voltage on the inductor current. Discussion on the design of PI controller to reduce the disturbance effects and improve current tracking is presented. To be able to carry out cascade control and to provide a steady reference inductor current, the bandwidth of the voltage loop cannot be too fast. This greatly affects the speed of response of the voltage loop and the disturbance rejection of the converter. However, with the addition of a dead-band relay on top of the PI controller on the primary voltage loop, the performance of the converter can be enhanced. Experimental examples are included to demonstrate the effectiveness of the proposed design scheme. The efficiency of the converter is 93% [Prodic et al., 2004]and the resultant total harmonic distortion of supply current is less than 2.9% at full load. Comparison with other fast controllers has also been made.

The main contribution of the controller is the simple design which includes a dead- band relay on top of the conventional double loop design, the speed of response of the converter and the disturbance rejection of the converter. With the introduction of the dead-band relay, the speed of response is greatly improved because any disturbances can

be settled in less than 20ms. Also, the disturbance rejection will be improved because the output voltage variations have been trapped by the width of the dead-band relay.

1.2 Problem Statement

AC–DC power conversion needs the output DC voltage to be well regulated with good steady-state and transient performances. The rectifier with a filter capacitor is cost effective, but it severely degrades the quality of the supply, thereby affecting the performance of other loads connected to it. Although, a large electrolytic capacitor suppresses the ripple from the output voltage, it introduces distortions to the input current and draws inrush current from supply. This introduces several problems, including a reduction of available power; the line current becomes non-sinusoidal which increases THD, and increases losses. This results in poor power quality, voltage distortion, and poor PF at input AC mains.

1.3 Purpose of the Study

This project is to examine a new cascade controller for the control of PFC boost converter. The proposed nonlinear cascade controller would outperform the conventional cascade controller with better disturbance rejection and faster speed of response. The study will also investigate and clarify on a new switching method which will improve the efficiency and hence the increased conduction loss of power devices would be reduced.

The objectives to achieve in this research are to:

- Design a new cascade controller for a non-linear power system to improve the disturbance rejection and speed of response of the conventional nonlinear cascade controller.
- Simulate the circuit designed with MATLAB/SIMULINK software to demonstrate the effectiveness of the proposed design scheme.

1.4 Research Questions

1. What non linear cascade controller is needed for a non-linear load system and to perform nearly unity power factor?
2. What modification could be done to the conventional nonlinear cascade controller to achieve a sinusoidal line current, decreasing Total Harmonic Distortion, and power losses and to attain a good power quality?

1.5 Limitation

Due to financial constraints, most effective drivers (Dual Topologies) of AC - DC was not selected.

1.6 Scope

The project is aimed at designing and simulating (using MATLAB/SIMULINK) the new cascade controller against the conventional cascade controller. Boost PFC converter-based on cascade controller control is being used in the proposed technique. The simplicity of the circuit configuration and the control structure mean that no regeneration back to the power supply is necessary. Besides, the input inductor can suppress the

surging input current, and the power switch is non-floating, so it is easy to design the driver circuit. A dead-band relay is introduced in the voltage loop to improve the disturbance rejection and speed of response of the PFC boost converter which makes it more accurate than other techniques, especially in transient operations, and when using distorted supply voltage, the input current has a sinusoidal waveform.

1.7 Project Organization

The project is organized as follows:

Chapter 2 describes the literature review. This includes journals, books and websites on power factor correction circuits where information was taken. Chapter 3 explains the Basic AC Modeling of boost converter and boost PFC converter-based on cascade controller. It also gives diagrammatic illustration on the proposed PFC control design for non-linear power system. Chapter 4 presents simulation result and discussions with and without power factor correction. Chapter 5Conclusions were drawn from the results obtained and possible suggestions for further improvement of the design were also given.

CHAPTER TWO

LITERATURE REVIEW

As per literature available till date various topologies have been developed for power factor correction. This chapter reviews the work done by various researchers in the field of different converter topologies and rectification circuits for power factor correction in DC-DC AND AC-DC system. The literature studied mainly deals with the following converter circuits:

- Modified single phase rectifier.
- Switching power converter with power factor correction (SPC-PFC).
- Single-Ended primary inductance converter (SEPIC) as front-ended converter.
- Repetitive proportional integral current controller for boost single phase ac-dc converter.
- PWM rectifier in three-phase static coordinate system and two-phase rotating coordinate system.

2.1 Converter and Rectification Circuits for Power Factor Correction

In this section different research papers corresponding to power factor correction circuit for High-Brightness Light Emitting Diodes (HB-LEDs) and other system, converter configuration and MATLAB simulation of converters are reviewed.

Jeyabharatlil, Veena and Rajaram (2005) proposed a sensor-less circuit with single–ended primary inductance converter (SEPIC) working as a power factor pre regulator

(PFP) in order to improve the power factor. It gives better current regulation and high power factor with simplified gate circuit achieved at low cost. The converter is suitable for DC and AC low power and high power application.

An improved non-isolated LED converter operating in Current Conduction Mode (CCM) with Power Factor Correction (PFC) and Average Current Mode Control (ACMC) for driving high power LED lamps by Xu et al, 2011. A laboratory proto-type with LUMILEDS emitter type LEDs is used to verify the feasibility of the proposed driver. From the measured results, it can be seen that the proposed LED driver achieves a power factor of 0.99 and a THD of 12.2% at input voltage 110 Vrms and a power factor of 0.96 and a THD of 10.4% at input voltage 220 Vrms. Many better performances such as high power factor, accurate average current control, low current harmonic and switch protection are confirmed and the experimental results match well with the analysis results

Jin, Leung, Man, He, Liang, Zhang, Qingxing, Du, Xiaomeng, and Chan (2013) presented a high power buck-boost switch-mode LED driver delivering a constant 350 mA with a power efficient current sensing scheme. An LED-current sensing circuit that consumes minimal power is proposed. The proposed sensing circuit senses LED-current by differentiating the voltage of the output capacitor and consumes less than 420μW power. It is implemented in a Buck-boost LED driver and the design is fabricated in AMS 0.35μm process. Measurement results confirm a reasonable sensing accuracy and line/load regulation. The maximum power efficiency is measured to be 92%. As the power consumption of the proposed LED-current sensing circuit does not increase

proportionally with the LED-current, the circuit is particularly useful when LED-current continues to increase in the future.

Enjeti, and Marines (1994) proposed a high performance single phase AC to DC rectifier with input power factor correction, by only having two semiconductors in the current path at any time; losses can be reduced over the conventional boost topology. Size and cost are also reduced by using fewer components and having the input inductor on the input ac side. The proposed topology, find it suitability for low and medium power application such as in power supplies and motor drives.

Hassan (2011) presented the theory and application of repetitive proportional integral current controller for boost single phase ac-dc converter with power factor correction (PFC). A repetitive controller which is inserted in series with the proportional integral (PI) controller shows very low crossover distortion of input current, low total harmonic distortion and very low tracking error when it was compared with the conventional proportional integral controller. Full analysis of proposed controller is given and Matlab/Simulink is used for simulation. The simulation results show the validity of the proposed control method.

Kwon, Shin and Rim (1997) presented the SRM drive system with the improved power factor and reduced harmonics. The system consists of the switching power converter with power factor correction (SPC-PFC), DC/DC converter and 3-phase inverter. AC/DC boost converter with SPC-PFC is operated as commented by the algorithm of power

factor correction. DC/DC converter is operated to meet dc-link voltage determined by speed command. Inverter applies the voltage to the winding of SRM in response to the position and current-chopping signals. The SPC-PFC is designed to produce the pure sinusoidal input current, improve the power factor, and reduce harmonics.

An LED lighting driver has been designed, including an integrated circuit with integral part and the buck converter topology with low-level switch and low-side sense resistor. The integrated circuit has been fabricated based on the CSMC 0.5μm 40V BCD process. In this way, the driver with high accurate output current and high efficiency can be obtained. The final result shows that the output current error is less than 1% and the efficiency is above 96%. Since a significant improvement has been obtained, the circuit is potentially applicable for future LED lighting (Jiang et al, 2014).

Simonetti, Sebatian and Uceda (1997) presented SEPIC and CUK converter working as a power factor pre-regulator (PFP) in discontinuous conduction mode (DCM). And analyzed the desirable characteristics of (PFP), the converter works as a voltage follower and theoretical power factor is obtained unity.

Consoli, Testa, Aiello, Gennara and Lo Presti (2001) presented an innovative converter topology based on C-dump converter configuration that is able to act as an active power factor controller. According to the features of the proposed circuit a conventional PFC stage is unnecessary to comply with the European standards on power quality, thus reducing the cost and the complexity of switched reluctance motor drives aimed to equip home appliances.

An improved non-isolated LED converter operating in Current Conduction Mode (CCM) with Power Factor Correction (PFC) and Average Current Mode Control (ACMC) for driving high power LED lamps. A laboratory proto-type with LUMILEDS emitter type LEDs is used to verify the feasibility of the proposed driver. From the measured results, it can be seen that the proposed LED driver achieves a power factor of 0.99 and a THD of 12.2% at input voltage 110Vrms and a power factor of 0.96 and a THD of 10.4% at input voltage 220Vrms. Many better performances such as high power factor, accurate average current control, low current harmonic and switch protection are confirmed and the experimental results match well with the analysis results (Xu et al, 2011).

A high efficiency LED (Light Emitting Diode) driver based on Buck converter, which could operate under a wide AC input voltage range (85V - 265V) and drive a series of high power LEDs, was presented in this paper. To verify the feasibility, a laboratory prototype is also designed and tested for an LED lamp which consists of 16 LUMILEDS LEDs in series. Experimental results show that a high efficiency of 92% at Ia = 350 mA can be achieved and the studied driver might be practical for driving high power LEDs. In the last, the over-all efficiency over 90% is gained through some experiments under variable input and output voltages and verifies the validity of the designed driver (Xu et al, 2011).

Gopalarathnam and Toliyat (2002) presented a new converter topology with a single ended primary inductance converter (SEPIC) front-end proposed for SR motor. It consist one switch in series with each motor phase. All the switches are grounded-referenced,

which simplifies their gate drive. In low voltage DC applications, it is capable of boosting the available input dc voltage to maximize the current regulated operation of the drive. For AC supply applications, it can be designed for operating either in DCM or in CCM depending on the power level, and high power factor can be obtained. The front-end converter performs the task of power factor correction as well as phase-de fluxing, thus keeping the component count low.

A new power-efficiency high-power LED driver that could regulate the average output current precisely by integrating the error voltage between reference voltage and sensing voltage is proposed. The performance of the new control technique was verified by time-domain simulation and tested on the experimental circuit board. Measurement results showed that the average output current is equal to the preset current 350mA, and the driver can be used in different input voltages cases such as 6V, 12 V and 24 V etc. The simulated waveform and results confirm that the proposed driver can get a reasonable LED average output current accuracy and good regulation. Besides, the new driver also provides protection to MOS switches (Xu et al, 2014).

Thiyagarajah (1990) in his paper introduced a boost topology with a high frequency inverter. The circuit consists of a boost converter in the front-end, a full –bridge inverter isolated by a high frequency transformer, and a secondary rectifier circuit. The front-end boost converter corrects the power factor, and the inverter in the second stage provides high frequency ac voltage which is converted into dc output voltage. This multistage power conversion topology lowers the overall converter efficiency, and the requirement

of additional hardware decreases the reliability of the converter. This topology is useful for applications requiring isolation between input and output, such as charges for electric vehicles.

Morimoto (1991) proposed the non- isolated drive system employs a non-isolated boost power factor correction converter as an input to the PWM inverter. It provides input PFC and high, stable, dc bus voltage, widening the field-weakening range in drive systems. The buck-boost cascaded converter based PWM inverter. The buck front end converter limits the input current to charge up the output capacitor smoothly and corrects the input power factor. The boost stage ensures inverter operation at low input voltages by a voltage step-up operation. The overall Efficiency of the variable speed drive system with one of these multi-stage converters is relatively low compared with the single converter based drive system.

Sahid, Yatim and A. H. M. (2011) presented a new bridgeless power factor correction circuit based on Single-Ended Primary Inductance Converter (SEPIC). The small-signal and steady state analysis of the proposed converter has been derived using Current Injection Equivalent Circuit Approach (CIECA) method. It is found that these models are vital in knowing the dynamic characteristics and the appropriate parameters of the proposed converter operated in DCM. The simulation results show that the proposed converter is able to work as a simple PFC circuit with the capability to regulate the output voltage over a wide range of load values and with universal input voltage condition.

A simple design method for power factor correction (PFC) boost converter is presented. A new nonlinear cascade controller was successfully implemented for the control of PFC boost converter. The controller settings can easily be obtained from the boost converter settings. The proposed nonlinear cascade controller outperforms conventional cascade controller with better disturbance rejection and faster speed of response. The controller has been shown to be robust against load changes. The resultant power factor is over 0.99, the total harmonic distortion of supply current is less than 2.9% and the efficiency of the converter is 93% at full load (Tsang et al, 2006).

Xue and He (2013) in their paper introduced the control strategy of unit power factor PWM rectifier in three-phase static coordinate system and two-phase rotating coordinate system, and the two control method are compared. The topology structure of the rectifier circuit is introduced and the double closed-loop control strategy in three-phase stationary coordinate system is analysed. For the deficiency of control strategy, the control strategy in two-phase synchronous rotating coordinate system is proposed. This makes the independent control of active current and reactive current to be realized. Theoretical analysis and simulation results show that the control in synchronous rotating coordinate system has better steady state performance.

Quanmin N. et al. proposes an energy balance model (EBM) for analyzing bifurcation and chaos phenomena of capacitor energy and output voltage when the converter parameter is varying, based on boost converter operating in discontinuous mode. It was found that the capacitor energy and output voltage dynamic behaviors exhibit the typical

period-doubling route to chaos by increasing the feedback gain constant K of proportional controller. The accurate position of the first bifurcation point and the iterative diagram of the capacitor energy with every K can be derived from EBM. Finally, the underlying causes for bifurcations and chaos of a general class of nonlinear systems such as power converters are analyzed from the energy balance viewpoint. Comparing with the discrete iterative model, EBM is simple and high accuracy. This model can be easily developed on the nonlinear study of the other converters.

2.2 Harmonic Standards

In view of the widespread use of power electronic equipment connected to utility systems, various national and international agencies have proposed limits on harmonic current injection to the system by this equipment, to maintain good power quality. As a result, the following standards and guidelines have been established that specify limits on the magnitudes of harmonic currents and harmonic voltage distortion at various harmonic frequencies. *(Power Quality Assurance Journal,* September/October (1995); Mohan et al, 1989).

a) IEC Harmonic Standard 555-2, prepared by the International Electrotechnical Commission, and accepted by its National Committees of the following countries: Austria, Australia, Belgium, Canada, Egypt, Finland, France, Germany, Hungary, Ireland, Japan, Korea (Republic of), Netherlands, Norway, Poland, Romania, South Africa (Republic of), Switzerland, Turkey, and the United Kingdom.

b) EN 60555-2, "The Limitation of Disturbances in Electricity Supply Networks caused by Domestic and Similar Appliances Equipped with Electronic Devices, “European

Norm prepared by Comite Europeen de Normalisation Electro technique, CENELEC. This in fact is an adoption of the IEC 555-2 standard to the CENELEC member countries, and will be same for all countries in the European Union (Cogger et al, 1994).

c) IEEE Standard 519-1992, "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems."

2.3 Continues Conduction Mode (CCM)

For medium and high power single-phase PFC, continuous conduction mode (CCM) is preferred due to its high efficiency and low current stress in semiconductor components. In the conventional CCM topology, there are two control loops. They are the voltage loop, which is used to regulate the output voltage, and the current loop, which is used for the control of the input current. PFC voltage loops are normally implemented with low bandwidth (Yang, Z. H. et al, 1998) in order to reduce the AC ripple on the output voltage, which distorts the input current waveform. However, in the case of step load change, the controller cannot response fast enough, and this leads to large voltage overshoot. In addition to the analogue based proportional–integral–derivative control, other advanced control methods, such as sliding mode control (Lopez, O. et al, 2001), fuzzy logic control (Chung, H. S. H. et al, 1999), and neural network control (Simonetti, D. S. L. et al, 1993), could also be employed to provide fast dynamic response while maintaining the stability of the converter system over a wide operating range. However, most of them are digital control and they require expensive and fast digital signal processors to implement. References (Prodic, A. et al, 2004; Orabi, M. et al, 2002)

present some results on the stability issues of PFC converters due to its nonlinear behaviours

To improve the speed of response and to improve the disturbance rejection of conventional analogue controlled boost converters, a proposed nonlinear deadband relay is added to the conventional controller to enhance the dynamic response. To facilitate low cost analogue nonlinear control, nonlinear cascade control of PFC boost converter is proposed. Simple proportional plus integral controllers can easily be designed based on the state average model of the boost converter. The overall design will compose of two control loops with the voltage loop outside the inner current loop. As long as the dynamics of the inner current loop is much faster than the outer voltage loop, cascade control can be implemented. To achieve a high power factor and low current THD, the bandwidth of the current loop has to be sufficiently fast to track the power frequency as well as its higher harmonics. At the same time, the current loop must have sufficient attenuation to reduce the effect of supply voltage and output regulated voltage on the inductor current.

CHAPTER THREE

METHODOLOGY

Among the three basic topologies, only the boost and the fly back are suitable for power-factor correction applications. The buck (step-down) configuration is excluded because its energy storage inductor is not at the input side. The boost topology is not without its problems at the low point (cusp) of a rectified sinusoid. However, this can be taken care of passively with the output capacitor. In contrast, it is rather difficult to assure a smooth transition between boost and buck twice every rectified cycle. It is a control issue. It is also an EMI (Electro-Magnetic Interference) issue. For those considerations, we focus on the boost PFC alone.

The boost PFC typically comes in the form of Figure 3, in which the boosted output, *vu (t)* is fed back and sampled. The sampled output is compared with a reference. Meanwhile, the switched line current is also sampled, *isen(t)*and compared against a reduced line voltage. Both the voltage error and the current error are multiplied. The product controls the power switch.

In general, the current loop has a wider bandwidth (fast). The voltage loop is therefore low in bandwidth (slow), and the boosted output voltage is expected to carry significant ripple at twice the line frequency.

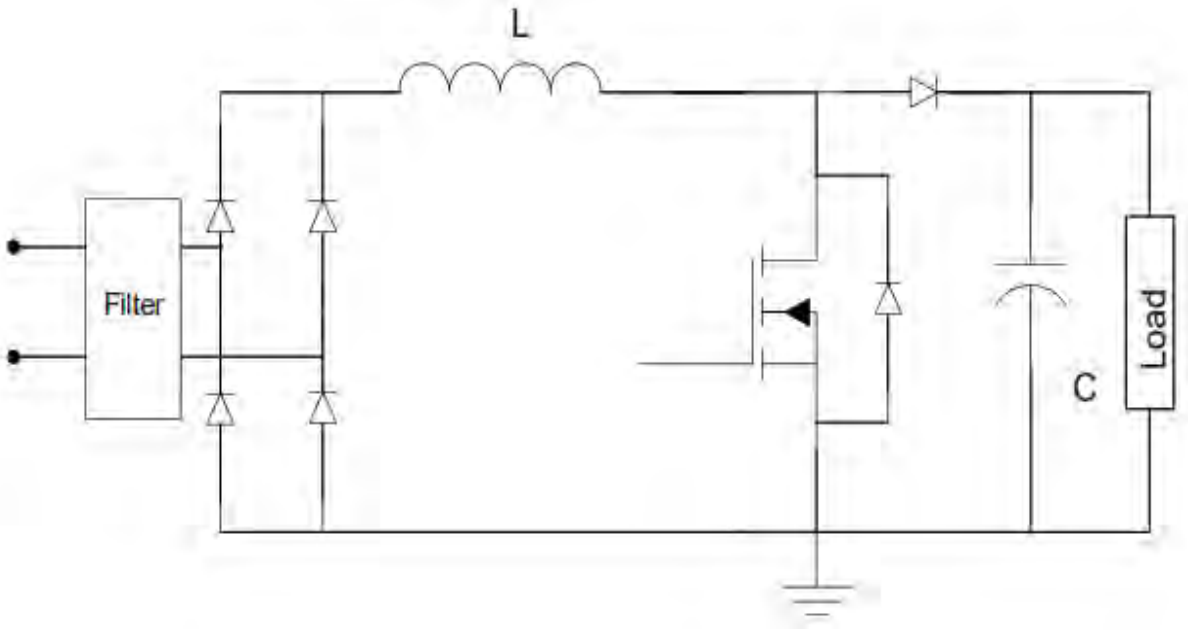

Figure 3.2: Boost - Power Factor Correction (PFC)

3.1 The Basic AC Modelling of Boost Converter

Figure 3.2 shows the AC model of the boost converter

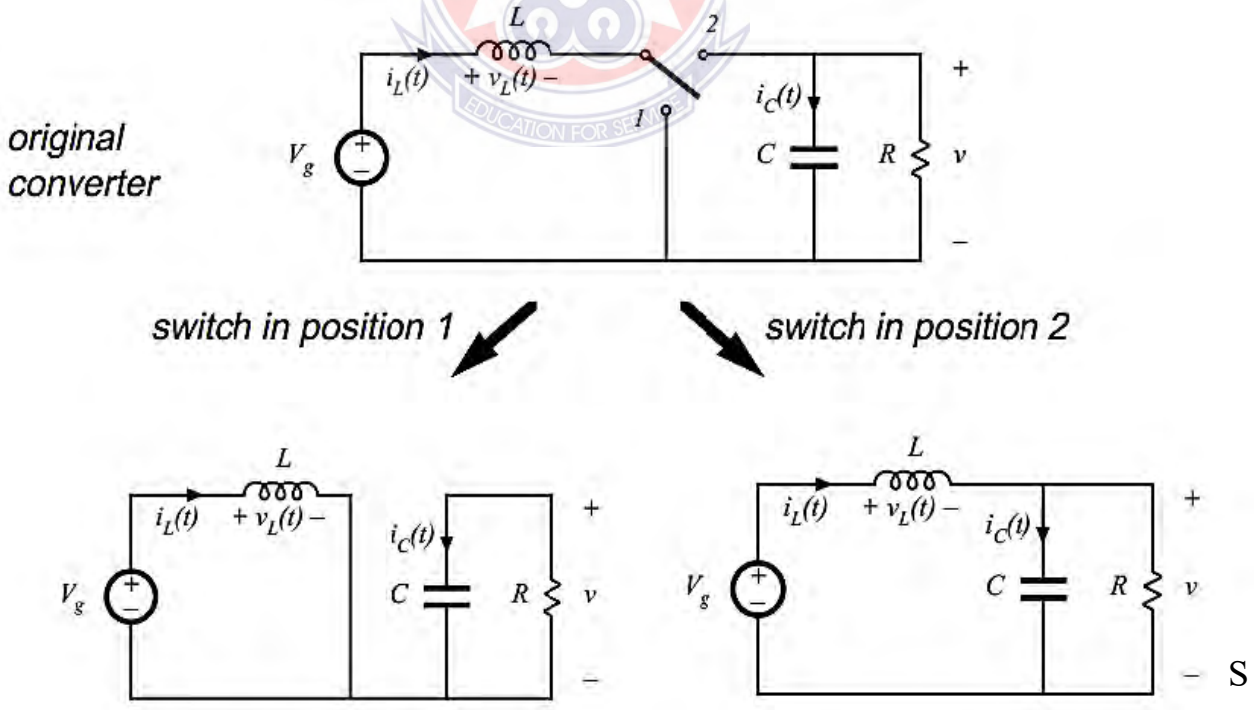

Figure 3.2: Boost converter

When the switch is in position 1, the inductor voltage and capacitor current are:

$$v_L(t) = L\frac{di(t)}{dt} = v_g(t) \qquad 3.1$$

$$i_c(t) = C\frac{dv(t)}{dt} = \frac{v(t)}{R} \qquad 3.2$$

Making the linear-ripple approximation in spite of replacing vg (t) and v(t) with their component $V_{g\ and}$ V and substituting them with their low-frequency averaged values $< v_g$ (t) $>_{Ts}$ and v(t) $>_{Ts}$ defined by the theorem:

$$< x(t) >_{Ts} = \frac{1}{T_S}\int_t^{t+Ts} x(\tau)d\tau$$

The equation thus become

$$v_L(t) = L\frac{di(t)}{dt} = < v_g(t) >_{Ts} \qquad 3.3$$

$$i_c(t) = C\frac{dv(t)}{dt} = -\frac{< v(t) >_{Ts}}{R} \qquad 3.4$$

Hence, during this sub interval, the inductor current and the capacitor voltage change with essentially constant slopes.

When the switch in position 2, its inductor voltage and capacitor current are:

$$v_L(t) = L\frac{di(t)}{dt} = v_g(t) - v(t) \qquad 3.5$$

$$i_c(t) = C\frac{dv(t)}{dt} = i(t) - \frac{v(t)}{R} \quad 3.6$$

Using small ripple approximation, and thus replacing it with averaged values.

$$v_L(t) = L\frac{di(t)}{dt} = < v_g(t) >_{Ts} - < v(t) >_{Ts} \quad 3.7$$

$$i_c(t) = C\frac{dv(t)}{dt} = < i(t) >_{Ts} - \frac{<v(t)>_{Ts}}{R} \quad 3.8$$

During second interval also, the inductor current and capacitor voltage change with the essentially constant slope.

3.2 Model of DC/DC Boost Converter

The state average model of a boost converter is given by

$$Li_L(t) = v_i(t) - (1 - d(t))v_o(t) \quad 3.9$$

$$C\dot{v}_o(t) = \big(1 - d(t)\big)i_L(t) - \frac{v_o(t)}{R} \quad 3.10$$

Where L is the inductance, C is the capacitance, R is the loading resistance, $i_L(t)$ is the inductor current, $v_o(t)$ is the output voltage, $v_i(t)$ is the rectified supply voltage, and $d(t)$ is the duty ratio respectively.

3.3 Cascade Controller Design

From 3.9 and 3.10, the boost converter can be decomposed to a voltage control loop and a current control loop.

3.3.1 Inner Current Loop Control

From 3.9, if the output DC voltage is assumed to be well regulated at U_o, the term $d(t)v_o(t)$ can be approximated as $U_o d(t)$. The current dynamics of 3.9 can then be approximated as

$$Li_L(t) = v_i(t) - v_o(t) + U_o d(t) \qquad 3.11$$

And a block diagram representation of the current loop control is shown in *figure3* where $i_r(t)$ is the reference inductor current that will be generated by the primary voltage loop PI controller. In order to eliminate the constant load disturbance contributed by the output DC voltage $v_o(t)$, and reduce the effect of supply voltage $v_i(t)$ on the inductor current $i_L(t)$, a proportional plus integral (PI) controller is included within the control loop. If the PI controller takes the form

$$\frac{d(s)}{I_r(s) - I_L(s)} = G_{PI_2}(s) = \frac{K_{P_2}S + K_{I_2}}{s} \qquad 3.12$$

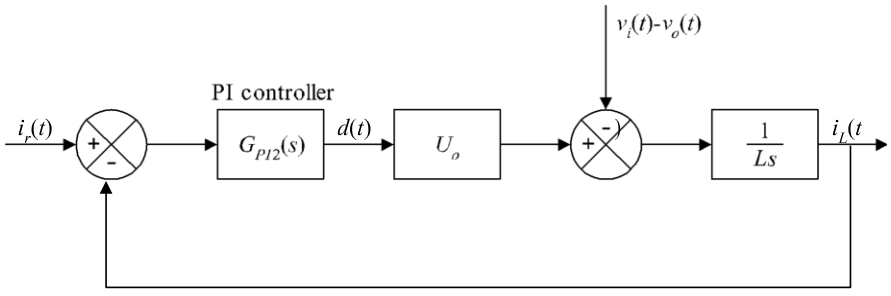

Figure 3.3: Current control loop

Where K_{P2} and K_{I2} are constants, the output inductor current becomes

$$I_L(s) = -\frac{s}{Ls^2 + K_{P_2}U_o s + K_{I_2}U_o}V_o(s) + \frac{s}{Ls^2 + K_{P_2}U_o s + K_{I_2}U_o}V_i(s) + \frac{(K_{P_2}s+K_{I_2})U_o}{Ls^2+K_{P_2}U_o s+K_{I_2}U_o}I_r(s) \quad 3.13$$

Where $I_L(s)$ and $I_r(s)$ are the Laplace transform of the inductor current $i_L(t)$, the reference current $i_r(t)$,$V_i(s)$, and $V_o(s)$ are the Laplace transform of the rectified supply voltage $v_i(t)$, output DC regulated voltage $v_o(t)$, *d(s)* is the Laplace transform of the duty ratio, and the Laplace variable, respectively. Notice that the output of 3.12 is the averaging of the PWM. From 3.13, the settings of K_{P_2} and K_{I_2} play an important role in the PFC boost converter as they will affect the rejection of the disturbances caused by $V_i(s)$ and $V_o(s)$ and the following of the reference current $I_r(s)$. In actual practice, $V_o(s)$ composed of a well regulated DC component and small ripples and $V_i(s)$ is in phase with the reference $I_r(s)$. The major concern in the current control loop is to eliminate the disturbance caused by the output DC voltage and try to track the reference current $I_r(s)$. Since there is an *s* in the numerator of (13), the DC components of $V_o(s)$ and $V_i(s)$ can be eliminated by the current loop controller. The reference current $I_r(s)$ is derived from the rectified supply voltage, the frequency content of the reference signal will compose twice the supply frequency and its higher harmonics. In order to track the reference current, the bandwidth of the current control loop has to be set as high as possible such that the gain and phase variations of the closed-loop control process up to 40th harmonics are small. If the undamped natural frequency ω_I of the current loop is set to$1/m$ times the switching frequency of the converter such that

$$\omega_I = -\frac{2\pi fs}{m} = \sqrt{\frac{K_{I_2} U_o}{L}}, \text{ m} \geq 4$$

where fs is the switching frequency of the converter, the required K_{I_2} is thus given by

$$K_{I_2} = -\frac{(2\pi)^2 f_s^2 L}{m^2 U_O} \qquad 3.15$$

If the current loop is set to be critically damped with damping ratio equal to 1

$$2\omega_I = \frac{K_{P_2} U_o}{L} \Rightarrow K_{P_2} = \frac{4\pi fsL}{mU_O} \qquad 3.16$$

Hence, with the current loop PI controller of 3.12 with settings of 3.15 and 3.16, the undamped natural frequency of the current loop will be $1/m$ times the switching frequency, and the current loop is critically damped. From 3.13, if the output voltage is well regulated at U_O, the dynamics of the current loop is independent of the loading resistor and the supply voltage.

3.3.2.2 Robustness Analysis

For the current control loop, the uncertainly is arisen from the output regulated voltage U_O. If there is a 20% increase in the output regulated voltage, from 3.14 the undamped natural frequency becomes $\sqrt{1.2}\,\omega_I$=1.0954ω_I and the damping ratio of the current loop becomes$\sqrt{1.2}$ =1.0954. When there is a 20% reduction in the output voltage, from 3.14 the undamped natural frequency becomes $\sqrt{0.8}\,\omega_I$=0.8944ω_I and the damping ratio of the current loop is $\sqrt{0.8}$ =0.8944. Even if there is 20% changes in the output regulated voltage, the current loop is still well under control with small changes in the

undamped natural frequency and damping ratio. In actual practice, the output voltage ripples will normally be less than 5% of the regulated voltage and the changes in the undamped natural frequency and damping ratio will be much less.

3.3.2 Primary Voltage Control Loop

From 3.10, the current term can be written down as

$$\big(1 - d(t)\big)i(t) = (1 - D - \tilde{d}(t))i(t) = (1 - D)i(t) - \tilde{d}(t)i(t)$$

Where D is the average duty ratio and $d(t) = D + \tilde{d}(t)$. For the design of the voltage control loop, the dynamics of the voltage loop is very much slower than the current loop and the net effect of $\tilde{d}(t)i(t)$ on the output voltage can be neglected because the frequency content of $\tilde{d}(t)i(t)$ is higher than the bandwidth of the voltage loop. If the inductor current $i_L(t)$ is taken as the control input to the converter, the transfer function between the output regulated voltage and the inductor current can be approximated as

$$G_v(s) = \frac{V_o(s)}{I_L(s)} = \frac{(1 - D)R}{RC_S + 1} \qquad 3.17$$

Consider a PI controller of the form

$$G_{PI_1}(s) = \frac{K_1(R_O C_S + 1)}{(1 - D_O)R_O s} \qquad 3.18$$

Where K_1,D_0, and R_O are constants ,applying to 3.17 with current reference derived from the rectified supplied voltage $V_i(s)$, the block diagram of the voltage control loop, shown in Figure4a where α is a constant. Assuming a steady state can be reached and the steady state output of the PI controller $W(t)$ is W_o, the block diagram of the voltage loop at the steady state can be approximate by Figure4b. The output DC regulated voltage can be approximated as

$$V_o(s) = -\frac{G_v(s)}{1+G_{PI_1}(s)G_v(s)}\left(\alpha W_o V_i(s) - \frac{W_O}{s}\right) + \frac{G_{PI_1}(s)G_v(s)}{1+G_{PI_1}(s)G_v(s)}V_r(s) =$$

$$\frac{(1-D)(1-D_o)RR_o\left(\alpha W_o V_i(s) - \frac{W_O}{s}\right)}{RR_oC(1-D_o)s^2+(R_o(1-D_o)+K_1RR_oC(1-D))s+K_1R(1-D)} +$$

$$\frac{K_1R(1-D)(R_oC_s+1)}{RR_oC(1-D_o)s^2+(R_o(1-D_o)+K_1RR_oC(1-D))s+K_1R(1-D)}V_r(s) \qquad 3.19$$

Where $V_r(s)$ is the Laplace transform of the reference voltage $v_r(t)$. The purpose of the PI controller here is to regulate the output DC voltage and to reduce the disturbance caused by the current reference, which is derived from the rectified supplied voltage. The DC components of $V_i(s)$ and $W_O$can easily be eliminated by the PI controller. Since $V_i(s)$ is derived from the rectified supply voltage, it will compose of a DC component, frequency component, which is two times the supply frequency, and its higher harmonics.

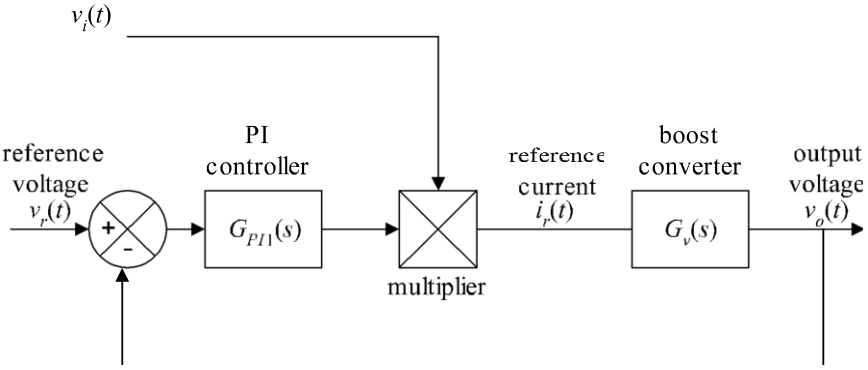

Figure 3.3a Voltage control loop

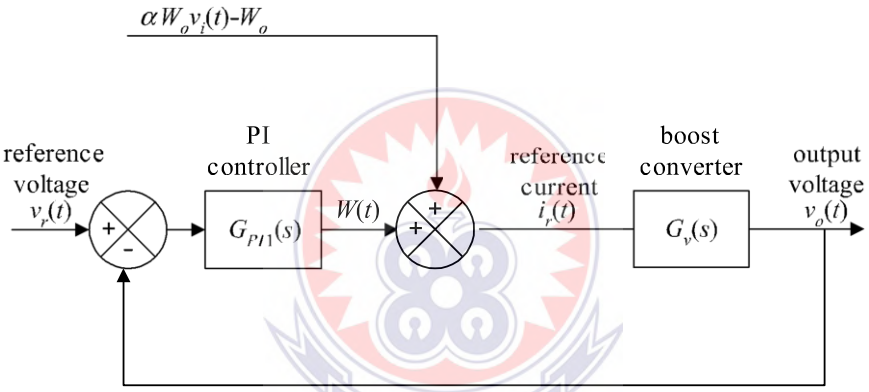

Figure 3.3b Voltage control loop: steady state approximation

To reduce the effect of the reference current on the output regulated voltage and to have a smooth PI output, the bandwidth of the voltage loop has to be very much less than two times the supply frequency, such that the fundamental frequency and its higher harmonics of the current reference are substantially attenuated by the voltage control loop. If the bandwidth of the voltage loop is too high, the disturbances will be reflected on the output DC regulated voltage. The voltage loop characteristic equation is given by

$$\Delta s = RR_oC(1-D_o)s^2 + (R_o(1-D_o) + K_1RR_oC(1-D))s + K_1R(1-D) \quad 3.20$$

With undamped natural frequency

$$\omega_n = \sqrt{\frac{K_1 R(1-D)}{(R_o RC(1-D_o)}} = \sqrt{\frac{K_1(1-D)}{R_o C(1-D_o)}} \qquad 3.21$$

And the damping ratio ζ governed by

$$2\zeta\omega_n = \frac{R_o(1-D_o) + K_1 R_o RC(1-D)}{R_o RC(1-D_o)} = \frac{1}{RC} + K_1 \frac{(1-D)}{(1-D_o)}$$

or

$$\zeta = \frac{1}{2\zeta\omega_n RC} = + \frac{K_1(1-D)}{2\zeta\omega_n(1-D_o)} \qquad 3.22$$

Clearly the undamped natural frequency ω_n is independent of the loading resistor R. Carrying out the design based on the nominal load with $R = R_o$ and $D = D_o$, the closed-loop system reduces to a first order system and the voltage loop characteristic equation becomes

$$\Delta s = s + K_1 \qquad 3.23$$

If the bandwidth of the voltage loop is set to $1/n$ times the supply frequency fv, the controller gain K_1 becomes

$$K_1 = \frac{2\pi f_v}{n} = + \frac{\gamma}{R_o C} \qquad 3.24$$

Where γ is a constant

3.3.2.3 Worst Case Analysis.

For the voltage control loop, the uncertainty is arisen from different loading conditions. To assess the robustness of the control design with 3.18 and 3.24, two extreme cases are tested. With the loading resistor approaches zero, from 3.22

$$2\zeta\omega_n = \infty \tag{3.25}$$

Implies that the system is well overdamped with $\zeta = \infty$. If the loading resistor approaches infinity,

$$2\zeta\omega_n \Rightarrow K_1 \Rightarrow \zeta = \frac{\sqrt{\gamma}}{2} > 0 \tag{3.26}$$

The two tests indicate that the system is well under control under different loading conditions because if the load current is above the nominal value, the system will be over damped resulting with a slower response system. Even if the load current is well below the nominal value, the damping ratio will not fall below 0.

3.2.2.4 Change of Duty Ratio

Under ideal conditions, the undamped natural frequency of 3.13 and the damping ratio of 3.14 with nominal load are given by

$$\omega_{n_i} = \frac{\sqrt{\gamma}}{R_o C} \tag{3.27}$$

and

$$\zeta_i = \frac{1+\gamma}{2\sqrt{\gamma}} \tag{3.28}$$

respectively. Different loading conditions may have a slightly different average duty ratio. If there is a +20% change in the ratio $(1-D)(1-D_o)$, under nominal loading condition, the undamped natural frequency of (13) becomes

$$\omega_{n_+} = \frac{\sqrt{1.2\gamma}}{R_o C} \tag{3.29}$$

And the damping ratio of 3.14 becomes

$$\zeta_+ = \frac{1+\gamma}{2\sqrt{1.2\gamma}} + \frac{0.2\gamma}{2\sqrt{1.2\gamma}} \tag{3.30}$$

The ratio $\frac{\zeta_+}{\zeta_i}$ is given by

$$\frac{\zeta_+}{\zeta_i} = \frac{1}{\sqrt{1.2}} + \frac{0.2\gamma}{2\sqrt{1.2\gamma}} \tag{3.31}$$

For small γ, the changes in the undamped natural frequency and damping ratio will be less than 10%. If there is a −20% change in the ratio $(1-D)(1-D_o)$, under nominal loading condition, the undamped natural frequency of 3.13 becomes

$$\omega_{n_-} = \frac{\sqrt{0.8\gamma}}{R_o C} \tag{3.32}$$

and the damping ratio of 3.14 becomes

$$\zeta_{-} = \frac{1+\gamma}{2\sqrt{0.8\gamma}} - \frac{0.2\gamma}{2\sqrt{0.8\gamma}} \qquad 3.33$$

The ratio ζ_{-}/ζ_i is given by

$$\frac{\zeta_{-}}{\zeta_i} = \frac{1}{\sqrt{0.8}} + \frac{0.2\gamma}{2\sqrt{0.8\gamma}} \qquad 3.34$$

For small γ, the changes in the undamped natural frequency and damping ratio will be around10%. The analysis indicates that with as much as 20% changes in the average duty ratio, the corresponding changes in the undamped natural frequency and the damping ratio are around 10%. This again shows the robustness of the controller settings using 3.18 and 3.24.

3.3.3 Nonlinear Voltage Loop Control

To reduce the effect of the current reference signal on the output regulated DC voltage, the band width of the voltage loop has to be limited well below the supply frequencyf_v, and this limits the value of the controller gain K_1. With low bandwidth and small K_1, the speed of response and the disturbance rejection of the system will both be low. However, the dynamics and disturbance rejection can be improved if dead band relay is coupled with the PI controller in the voltage loop. Bang-bang control is seldom used in control systems because of the high frequency chattering in the outputs. However, the chattering can be removed by introducing a dead zone in the relay. *Figure 5* shows the dead band relay and the describing function for a dead band relay is given by

$$N(X) = \frac{4M}{\pi X}\sqrt{1 - \left(\frac{\varepsilon}{X}\right)^2} \qquad 3.35$$

Where X is the input amplitude, M is the relay output amplitude, and 2ε represents the dead bandwidth. *Figure 6* shows the block diagram of the voltage control loop when dead band relay is coupled with the PI controller. The derivation of current reference is taken out from the block diagram because it can be regarded as external disturbance and it is excluded in the stability analysis of the voltage control loop. It is also assumed that the current loop dynamics is very much quicker than the voltage loop such that it can be ignored in the analysis. The characteristic equation for the closed-loop system shown in *Figure 3.5* is given by

$$1 + (N(X) + G_{PI_1}(s))G_v(s) = 0$$

or

$$\frac{G_v(s)}{1 + G_{PI_1}(s)G_v(s)} = -\frac{1}{N(X)} \qquad 3.36$$

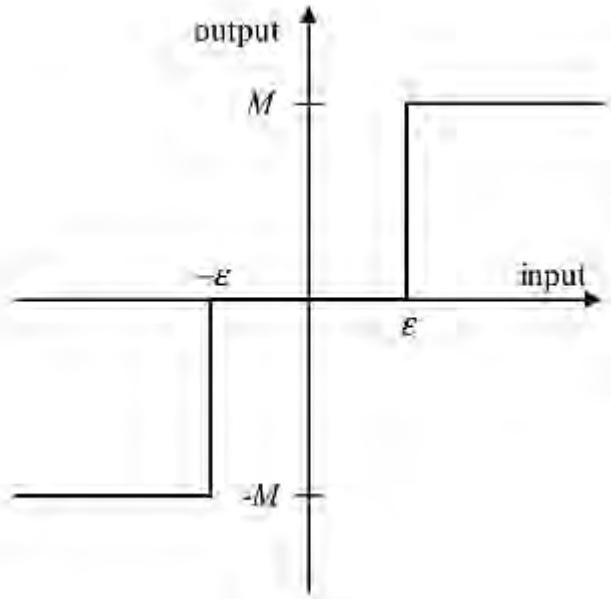

Figure 3.4 Deadband relay

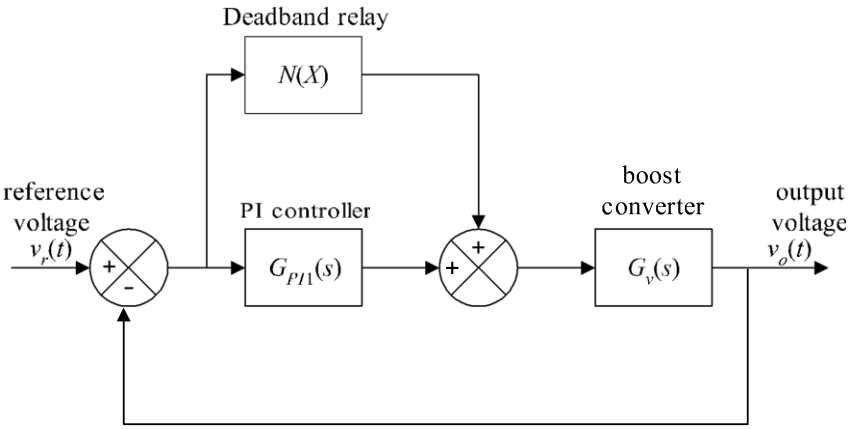

Figure 3.5 Voltage control loop and deadband relay

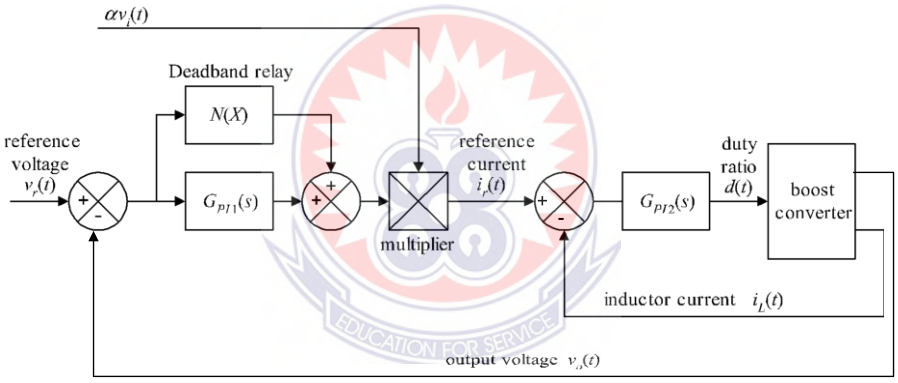

Figure 3.6 Nonlinear control of PFC boost converter

As long as the Nyquist plot of $G_v(s)/1 + G_{PI_1}(s)G_v(s)$ do not cut across $-1/N(X)$, limit cycle oscillation can be avoided. The design of $G_{PI_1}(s)$ guarantees the stability of the original voltage control loop shown in *Figure 6*, $1 + G_{PI_1}(s)G_v(s)$ only includes roots on the left half of s-plane. The minimum phase property of $G_{PI_1}(s)$ and $G_v(s)$ also results in a minimum phase property in $G_v(s)/1 + G_{PI_1}(s)G_v(s)$.As$G_v(s)$ is a first order system, the system order of $G_v(s)/1 + G_{PI_1}(s)G_v(s)$ is two. Because of the minimum phase

property, the frequency response plot of $G_v(s)/1 + G_{PI_1}(s)G_v(s)$ lies within the third and fourth quadrants of the Nyquist plot. The Nyquist plot of$-1/N(X)$ lies on the negative real axis. Since $G_v(s)/1 + G_{PI_1}(s)G_v(s)$ never cut across the negative real axis, limit cycle can be avoided and the closed-loop system is stable. Also, there is a lot of freedom in the design of the dead band relay. The introduction of the dead band relay in the control loop has the following effects. If the error voltage is less than the threshold ε, the relay will have no action and the PI controller will dominate the control process. However, if the error voltage is larger than the threshold ε, the PI controller will combine its output with the full magnitude relay output to improve the speed of response and disturbance rejection of the system. The selection of ε can be obtained from the disturbance part of 3.19. With rated supply current under the ideal case, the transfer gain between the reference current and the output DC voltage at twice the supply frequency can be obtained. E is then set to a value slightly above the peak magnitude of the output ripple output at full load. The block diagram of the proposed non-linear control scheme is shown in *Figure 7*.

CHAPTER FOUR

DISCUSSION AND RESULT

MATLAB/SIMULINK of PFC boost converter had been design with L=500μH ,C=470μF, nominal supply voltage was 100Vrms, and the supply frequency was $f_v = 50Hz$. The output regulated voltage was set to $U_o = 180$ V and the nominal loading resistor R_o was 200Ω. The nominal duty ratio D_o was defined as U_o/rms of $v_i(t) = 1/1 - D_o = 180/100$ and α was set to 0.0033 such that the peak value of $\alpha v_i(t)$ was about 0.47V. The setting of α was to make sure $\alpha v_i(t)$ is less than unity such that the multiplier output would not be easily saturated. The switching frequency was set to $f_s = 100kHz$, the undamped natural frequency of the current loop was set to 1⁄5 of the switching frequency with m=5 and the damping ratio of the current loop was set to 1. From 3.15 and 3.16, the current loop PI controller of 3.12 became

$$G_{PI}(s) = 0.6981 + \frac{43865}{s} = 0.6981\left(1 + \frac{62832}{s}\right) \quad 3.37$$

Attenuation of more than 40dB has been achieved between the regulated output voltage and the inductor current. The attenuation between the supply voltage and the inductor current is the same. These demonstrate there are good attenuation on the supply voltage and regulated output voltage and the two voltages will have little effects on the inductor current. The Bode plots for the transfer function between the reference current and the inductor current under ideal conditions are shown in Figure8. The gain variation and phase shift up to 2kHz are negligible, which means the inductor current can follow the reference current very well up to 2kHz. For the voltage control loop, the bandwidth was

set to 1⁄5 of the supply frequency f_v and the voltage loop PI controller of 3.10 became.

$$G_{PI}(s) = 0.0532 + \frac{0.5655}{s} = 0.0532\left(1 + \frac{10.63}{s}\right) \quad 3.38$$

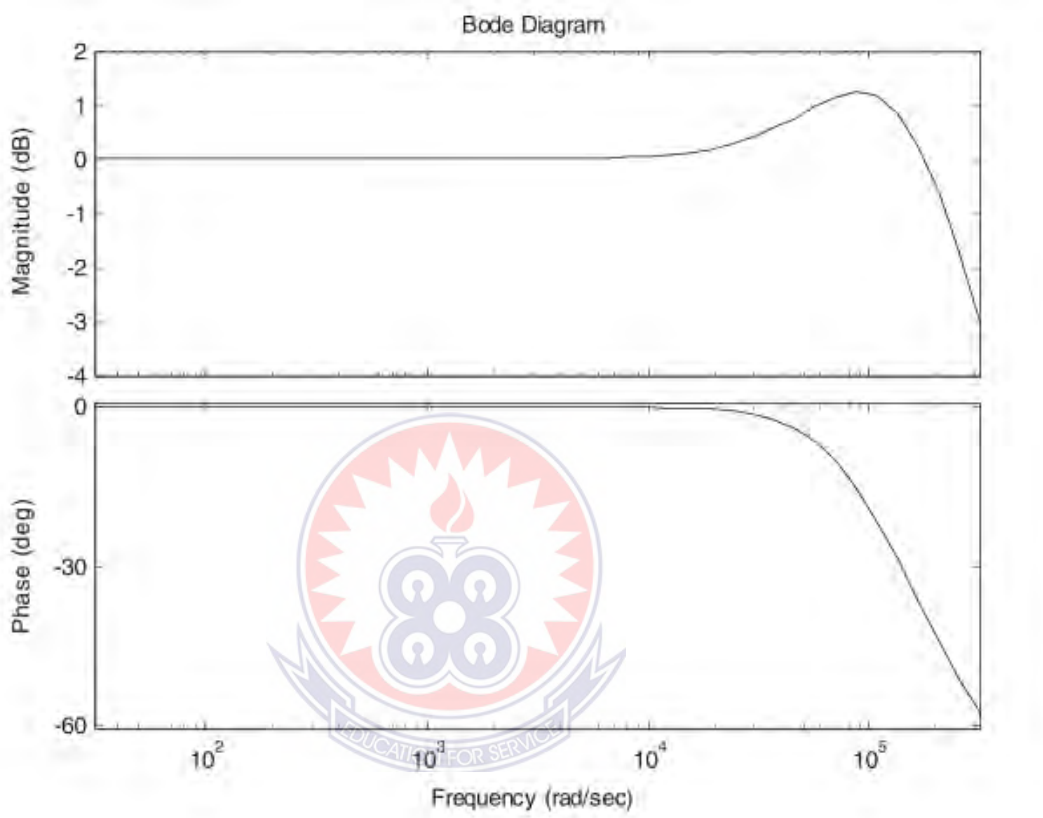

Figure 4.1 Bode plots for the transfer function between the reference current and inductor current

Frequency components of 100Hz and above will have at least 20dB attenuation. Hence, frequency components of 100Hz or above will be attenuated by the control loop and the output response of the voltage loop PI controller will be very steady with little influence from the reference current. The steady output of the voltage loop PI controller warrants a good generation of the reference current.

From 3.11, the gain between the reference current and the output DC voltage under nominal load conditions at 100Hz is 1.87V/A. If the rated current is taken as 1.62A, the peak output ripple voltage is 4.28V. The steady state response of the PFC boost converter under nominal load conditions is shown in *Figure 9*. The peak to peak variation in the output DC regulated voltage was about8V. Hence, the settings for the dead band relay were ε=4.5V and M=10. Theoretically there is no limit on the relay output magnitude. However, in order not to excite the unmodelled dynamics of the converter, the setting of the relay output magnitude M is set to about 10times the nominal current. The hardware implementation for the nonlinear PFC boost converter is shown in *Figure 10*.

To demonstrate the performance of the controller under different working conditions, different supply voltages and loading conditions were tested. Table1 shows the performance of the nonlinear controller obtained from the Fluke 41B power harmonics analyzer under different supply voltages and loading resistors. The steady performance of the proposed PFC boost converter was comparable to commercial PFC boost converters. To demonstrate the performance of the controller with constant power load, the output of the boost converter was connected to a DC – DC converter. The output voltage was stepped down to 15V and the switching frequency of the DC – DC converter as 80kHz. Table 2 shows the performance of the nonlinear controller with constant power load of 38W and 63W. Clearly the results are comparable to results with linear resistors.

4.1.1 Simulation result (Steady-state response)

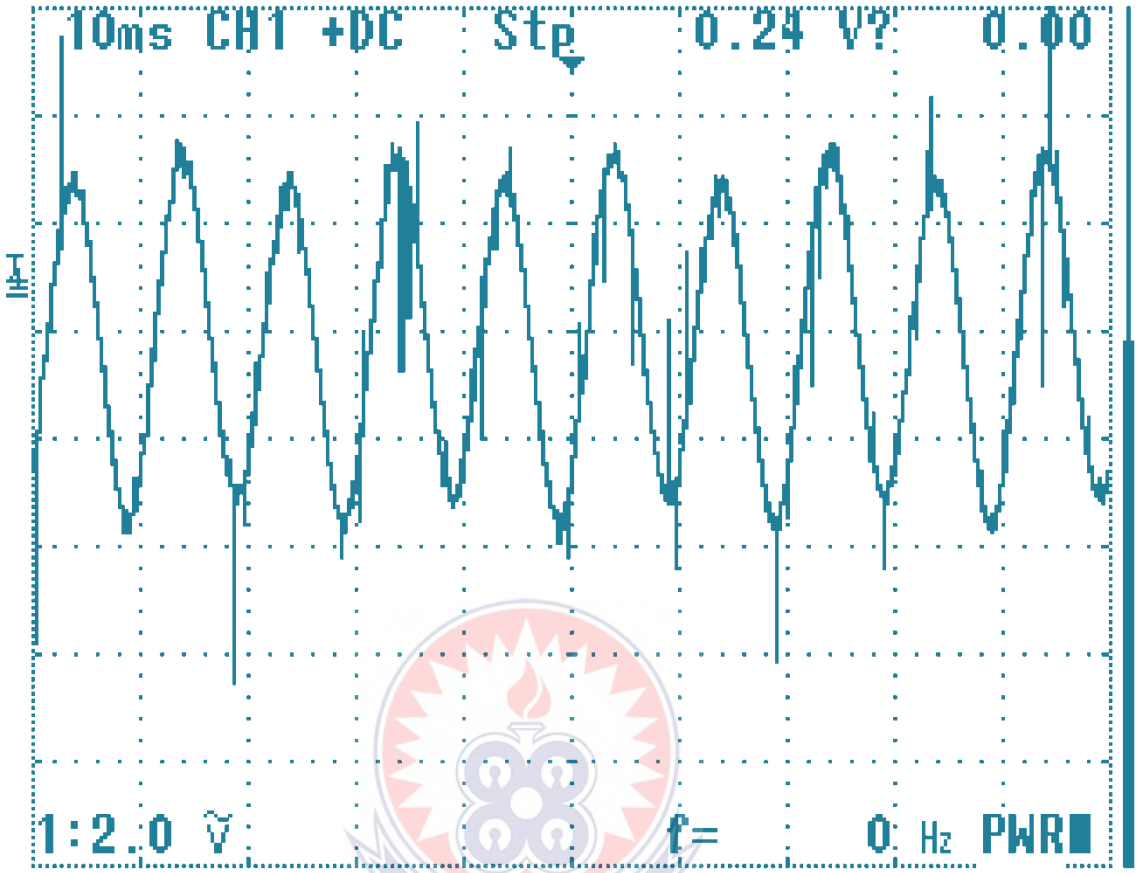

Figure 4.2 Steady state response of PFC boost converter under norminal load

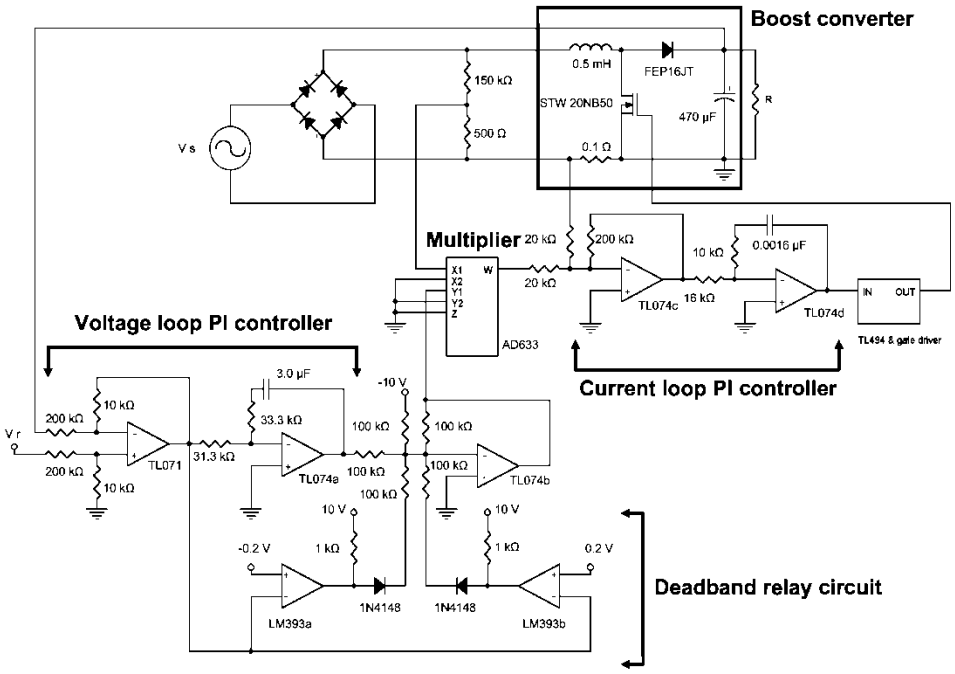

Figure 4.3 Circuit diagram of the nonlinear controller for the PFC boost converter

Table 4.1: Performance of the nonlinear cascade controller with different supply voltages and loading conditions

Supply Voltage (Vrms)	Loading Resistor (Ω)	Supply current (Arms)	Power (W)	Current THD	Power factor
80	200	2.35	187	3.4%	1
100	200	1.87	186	2.9%	1
120	200	1.47	175	2.6%	1
80	850	0.62	49	5.5%	0.99
100	850	0.46	45	8.0%	0.99
120	850	0.37	43	10.6%	0.98

Table 4.2: Performance of the nonlinear cascade controller with constant powerload

Supply voltage (Vrms)	Supply Current (Arms)	Power (W)	Current THD	Power factor
100	0.63	63	5.2%	1
100	0.4	38	9.2%	0.99

4.1.2 Simulation result (Performance of linear and nonlinear cascade controllers):

(a)

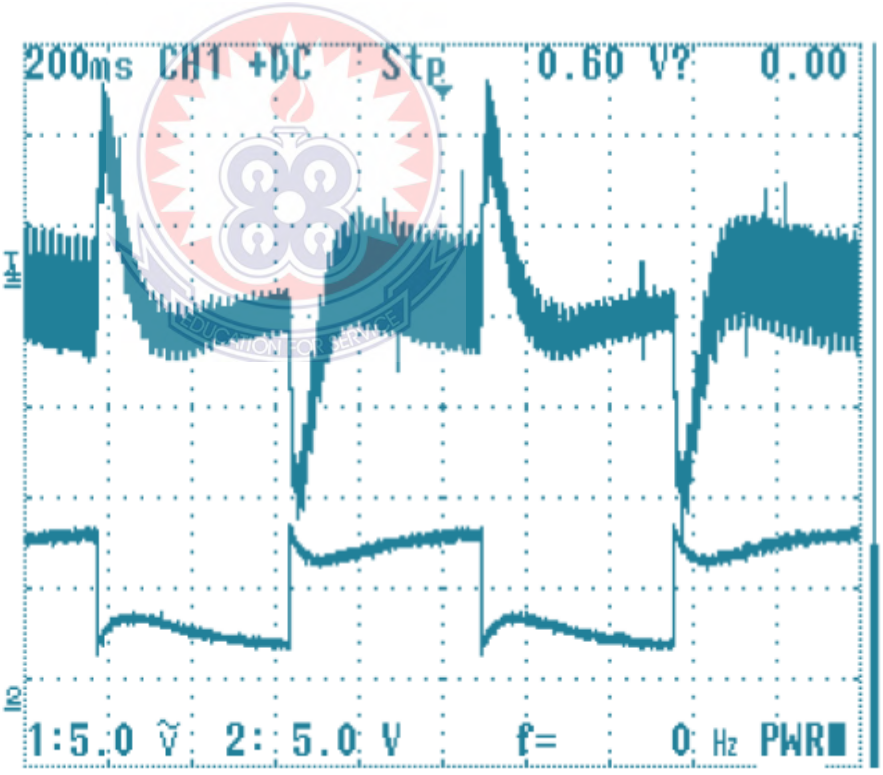

Figure 4.4: Performance of linear and non linear cascade controllers: linear controller with changing linear resistor

(b)

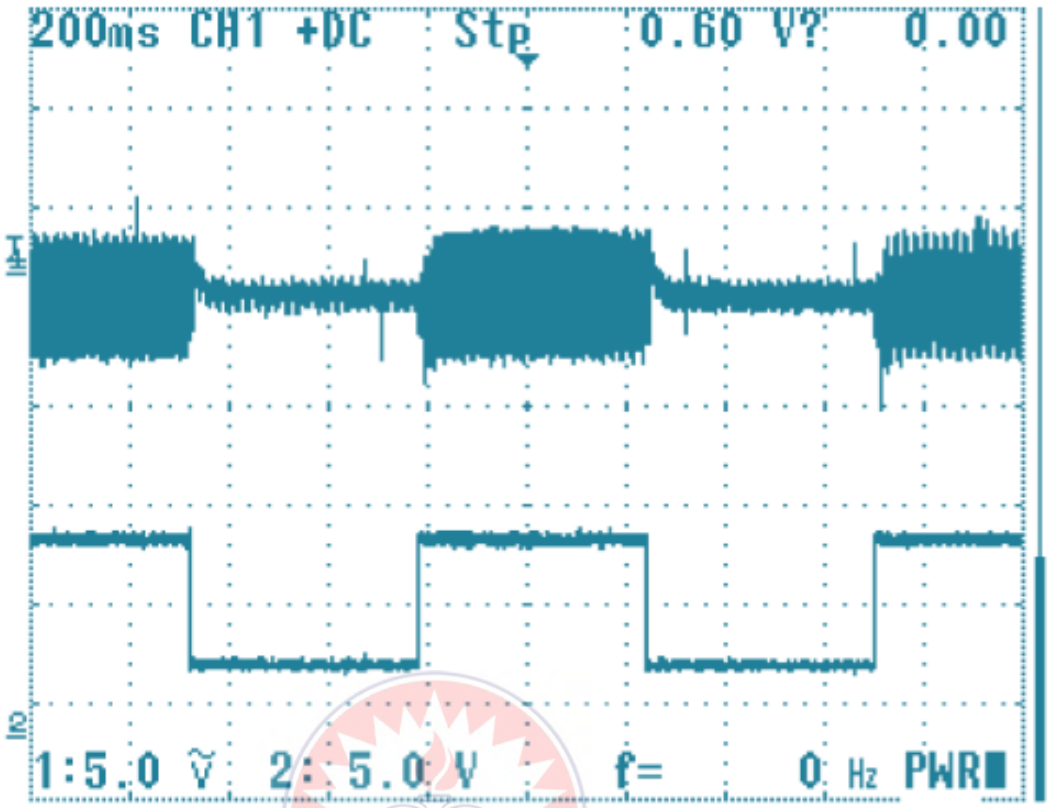

Figure 4.5: Performance of linear and nonlinear cascade controllers: nonlinear controller with changing linear resistor

(c)

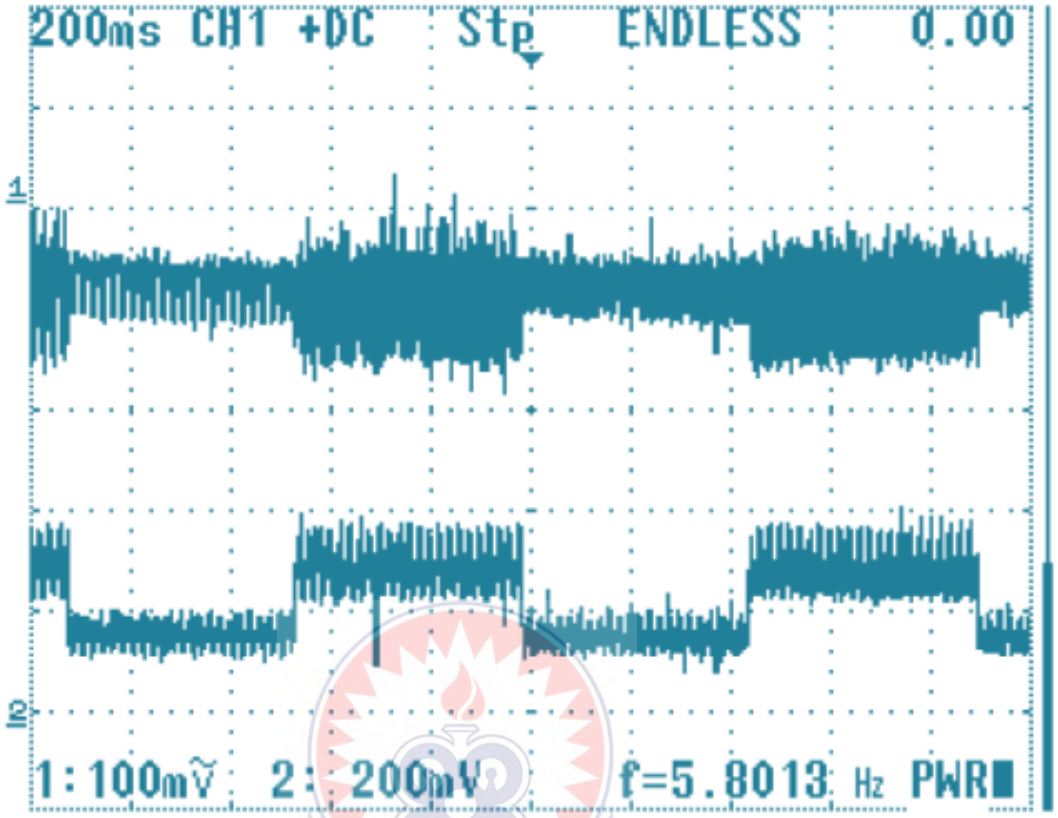

Figure 4.6 Performance of linear and non linear cascade controllers: non linear controller with changing constant powerload

4.1.3 Discussion

To demonstrate the effectives of the proposed controller over conventional controller, the load was switched between 200Ω and 850Ω and the supply was fixed at 100Vrms. *Figure 4.4* shows the performance of the conventional cascade control without the dead band relay with channel 1 indicating the AC coupled DC output regulated voltage and channel 2 indicating the relative current demand of the load. The disturbance on the output regulated voltage went as high as 12V and it took around 200ms to settle down. *Figure 4.5* shows the performance of the proposed nonlinear cascade controller with the

same load demand. The disturbance on the output regulated voltage was unnoticeable and it took less than 20ms to settle down. Clearly the disturbance rejection and speed of response of the proposed nonlinear cascade controller was better than the conventional cascade controller. *Figure 4.4 and Figure 4.5* have an AC waveform equal zero, f = 0, because the AC waveform has a DC component. The average voltage would be equal to the DC voltage instead, because opposite peaks cancel each other leaving only the DC component. *Figure4.6* shows the performance of the proposed controller with constant power load switched between 38W and 63W. Again, the disturbance on the output regulated voltage was unnoticeable and it took less than 20ms to settle down, whereas the settling time of converter proposed by Eissa, Leeb, Verghese & Stankovic, (1996) took over 30ms.

The steady-state supply voltage and current waveforms shows clearly that the input current is in phase with the input voltage for boost PFC converter using the proposed technique.

The steady-state simulation results of input current and its harmonic spectrum for the proposed technique also clearly shows that the proposed technique has a nearly sinusoidal input current waveform with low harmonic contents, within a range of 10.6 to 2.6% and high power factor, within a range of 0.98 to 1 which proves the efficiency of the proposed technique.

The rectified voltage, rectified current and the reference current waveforms which shows that the rectified current is always very close to the reference current for the proposed technique.

For the load voltage and current waveforms, it is noted that the load voltage and current have a nearly DC value with very small ripples that do not have any effect on its operation.

For the steady-state input voltage and current waveforms for the proposed technique under distorted supply voltage, it is shown that the input current has a sinusoidal waveform and being in phase with the input voltage.

CHAPTER FIVE

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

A new nonlinear cascade controller has been successfully implemented for the control of PFC boost converter. The controller settings can easily be obtained from the boost converter settings. The proposed nonlinear cascade controller outperforms conventional cascade controller with better disturbance rejection and faster speed of response. The controller has been shown to be robust against load changes. Robustness analysis of the cascade controller against load changes was presented

5.2 Recommendation

The proposed nonlinear cascade controller is very practical. The implementation is easy and the cost is low. As major building blocks for the controller are already available in off – the – shelf chips such as UC3854, the additional cost for the proposed controller is the dead band relay, which can easily be integrated into conventional chips in future. Regarding the efficiency of the boost converter, the proposed controller is as good as any commercially available product. However, the efficiency can be improved by incorporating a new switching method. Under the method proposed by Li & Ruan, (2004), the MOSFET's on-time and the current magnitude can be shortened. As a result, the efficiency will be increased because the conduction loss of power devices can be reduced.

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